UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,827	10/23/2001	Ming-Dou Ker	NAUP0324USA	6934

27765 7590 10/28/2003

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
KITOV, ZEEV	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,827	KER ET AL.	
	Examin r	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 6 recites the limitation "the first ESD protection circuit", while in Claim 8 "the second ESD detection circuit" includes all the same elements as the first ESD protection circuit of Claim 6. For purpose of examination the Claim 6 limitation was interpreted as ""the first ESD detection circuit".

Objection

The claims are objected to because the claims should have subscripts attached to the letter to which they are supposed to be applied. For instance Claim 1, lines 2 – 3, the subscript is carried over to the next line. It makes the text difficult to read. The typing of the Claims should be corrected.

Abstract

Applicant is reminded of the proper format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. Appropriate correction is required.

1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 34 is rejected under 35 U.S.C. 102(a) as being anticipated by Ker 3 et al. (US 6,144,542). Ker 3 et al. disclose all the elements of the claim including a power-rail ESD clamp circuit for use with mixed voltages, which is electrically connected between a Vss power terminal and a Vdd power terminal, the power-rail ESD clamp circuit including a plurality of sub power-rail ESD clamp circuits (elements A and B in Fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 et al. (US 5,576,557) in a view of Smith (US 6,049,119).

Ker 1 et al. disclose most of the Claim 1 elements including an ESD protection circuit having an I/O pad and an internal circuit (elements 2 and 3 in Fig. 1), a Vss and a

Vdd power terminals, a first ESD-detection circuit connected between the I/O buffering pad and the Vss power terminal (element M2 in Fig. 1); a P-type silicon controlled rectifier (elements Q3 and Q4 in Fig. 1) including a first lateral silicon controlled rectifier (SCR) and a P-type trigger node (node 18 in Fig. 1), an anode and a cathode of the P-STSCR being electrically connected to the I/O buffering pad and the Vss power terminal respectively; a second ESD-detection circuit electrically connected between the I/O buffering pad and the Vdd power terminal (element M1 in Fig. 1); and an N-type silicon controlled rectifier including a second lateral SCR (elements Q1 and Q2 in Fig. 1) and an N-type trigger node (node 13 in Fig. 1), a cathode and an anode of the N-STSCR being electrically connected to the I/O buffering pad and the Vdd power terminal respectively.

However, they do not disclose the P-type and N-type substrates. The P-type and N-type trigger nodes were identified according to a polarity of triggering voltage. As to P-type and N-type substrates, according to Ker 1 et al., (col. 4, lines 10 - 16, col. 10, lines 1 – 8), the ESD protection circuit is compatible with both N-type well/P-type substrate and P-type well/N-type substrate, as well as twin well fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 1 et al. solution by using P-type or N-type substrate according to Ker 1 et al., because a criticality of selection of particular type of the substrate was not disclosed, and additionally, the reference states (col. 4, lines 10 - 16, col. 10, lines 1 – 8), it is not critical, a selection of particular type of the substrate is a matter of designer convenience, rather than element of a novelty.

Additionally, they do not disclose substrate-triggered ESD protection elements. Smith discloses the substrate-triggered ESD protection elements (element 13 in Fig. 3, col. 5, line 50 – col. 6, line 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 et al. solution by adding the substrate-triggering according to Smith, because as Smith states (col. 2, lines 12 – 25), the substrate-triggering helps to lower the trigger voltage, which as well known in the art is essential for protection circuits designed for use with low supply voltage.

Regarding Claim 2, Ker 1 et al. disclose the P-STSCR in the ESD protection circuit including a p-type substrate with N-wells (see Fig. 2), a first N-well diffusion region and a first P^+ diffusion region in P-type substrate used as the cathode of the P-STCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 28 and 27 in Fig. 2) in the N-well (element 23 in Fig. 2) used as the anode of the P-STCR, the second P^+ diffusion region, the N-well, the P-substrate and the first N^+ diffusion region forming the first lateral SCR.

Regarding Claim 3, Ker 1 et al. disclose a circuit wherein in response to a positive voltage pulse at the I/O buffering pad, the first ESD detection circuit produces a first trigger current flowing into the P-type trigger node of the P-STSCR triggering the first lateral SCR in the P-STSCR to enter a latch state, the latch state turning on the P-STSCR so that a current incurred from the positive voltage pulse is discharged to the Vss power terminal (col. 4, line17 – col. 7, line 54).

Regarding Claim 4, Ker 1 et al. disclose the circuit wherein the N-STSCR in the ESD protection circuit including a P-type substrate with N-wells (see Fig. 2), a first N^+ diffusion region and a first P^+ diffusion region in P-type substrate uses as the cathode of the N-STSCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 26 an 25 in Fig. 2) in the N-well (element 21 in Fig. 2) for use as the anode of the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

Regarding Claim 5, Ker 1 et al. disclose the circuit wherein in response to a negative voltage pulse at the I/O buffering pad, the second ESD detection circuit produces a second trigger current flowing into the N-type trigger node of the N-STSCR triggering the second lateral SCR in the N-STSCR to enter a latch state turning on the N-STSCR so that current incurred from the negative voltage pulse is discharged to the Vdd power terminal (col. 4, line17 – col. 7, line 54).

Regarding Claim 7, Ker 1 et al. disclose the circuit wherein the NMOS (element (element M2 in Fig. 1) enhances the first trigger current so as to accelerate the triggering of the P-STSCR.

Regarding Claim 9, Ker 1 et al. disclose the circuit wherein the PMOS (element M1 in Fig. 1) enhances the second trigger current so as to accelerate the triggering of the N-STSCR.

Claims 6, 8, 10, 12 and 14 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 et al. in a view of Ker 2 et al. (US 5,959,820). As was stated

above, Ker 1 et al. disclose all the elements of Claim 1. However, regarding Claims 6 and 8, they do not disclose the first and second ESD detection circuits having a resistor, a capacitor, a zener diode, a diode string or an NMOS. Ker 2 et al. disclose the ESD detection circuit having the resistor and capacitor (elements R and C in Fig. 15a and 15b), the zener diode (shown in Fig. 16e), a diode string (shown in Fig. 16b) and NMOS (part of element 206 in Fig. 16a and 16b). All these elements are well known and widely used in the ESD protection circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 1 et al. circuit by adding the resistor and capacitor, the zener diode or the diode string according to Ker 2 et al., because as well known in the art, presence of the RC element in the ESD detection circuit makes the ESD protection element reacting to a front edge of the ESD event and therefore faster than otherwise, while the zener diode or string of the diodes set a threshold of the SCR firing.

Regarding Claims 10, Ker 2 et al. disclose the fist ESD detection circuit including a third resistor with a third capacitor (elements R and C in Fig. 15a) a first inverter (element 206 in Fig. 15a), an input node of the first inverter electrically connected to the Vdd power terminal and the Vss power terminal through the third resistor and the third capacitor respectively, an output node of the first inverter electrically connected to the P-type trigger node of the P-STSCR (elements PCLSCR in Fig. 15a).

As per Claim 12, Ker 2 et al. disclose the fist ESD detection circuit including a third resistor with a fourth capacitor (elements R and C in Fig. 13a) a second inverter (part of element 204a in Fig. 13a), an input node of the first inverter electrically

connected to the Vdd power terminal and the Vss power terminal through the third resistor and the third capacitor respectively, an output node of the first inverter electrically connected to the P-type trigger node of the N-STSCR (elements NCLSCR in Fig. 13a).

Regarding Claim 11, in the ESD protection circuit of Ker 1 et al. modified according to Ker 2 et al., when a positive ESD voltage pulse is applied to the I/O buffering pad, the first inverter (element 206 in Fig. 15a) is charged by the positive ESD voltage pulse to generate a third trigger current at the output node of the first inverter, the third trigger current flowing into the P-type trigger node of the P-STSCR (elements PCLSCR in Fig. 15a) to trigger the fist lateral SCR, the first lateral SCR entering a latch state in response to the third trigger current and quickly turning on the P-STSCR so that current incurred from the positive voltage pulse is discharged to the Vss power terminal.

Regarding Claim 13, in the ESD protection circuit of Ker 1 et al. modified according to Ker 2 et al., when a negative ESD voltage pulse is applied to the I/O buffering pad, the first inverter (part of element 204 in Fig. 13a) is charged by the positive ESD voltage pulse to generate a third trigger current at the output node of the first inverter, the third trigger current flowing into the P-type trigger node of the P-STSCR (elements NCLSCR in Fig. 13a) to trigger the fist lateral SCR, the first lateral SCR entering a latch state in response to the third trigger current and quickly turning on the N-STSCR so that current incurred from the positive voltage pulse is discharged to the Vdd power terminal.

Regarding Claim 14, it differs from Claim 1, rejected accordingly by its requirement of plurality of stacked SCR's replacing single SCR's and functional limitations for values of holding voltage levels. Ker 2 et al. disclose the first stacked SCR (elements PCLSCR in Fig. 15a) and the second stacked SCR (elements NCLSCR in Fig. 13a) both including a plurality of the same type SCR's.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 et al. solution by replacing the single PSCR and NSCR by their stacked counterparts according to Ker 2 et al., because as Ker 2 et al. state (col. 3, lines 50 - 55), such solution has a high bypassing ability without latchup risk. The stacked LVTSCR can provide the CMOS IC with effective ESD protection but without accidental triggering on by the overshooting or undershooting noise pulses in the system applications.

As to the holding voltage levels, as well known the art, the threshold levels for switching devices should be such that an information signal can come through, while the noise is rejected. The recited noise rejection capabilities of the first and second stack of SCR's are common noise rejection requirements for the switching circuit. The SCR's are to be switched by the ESD detection signals, but must be immune to the noise. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 et al. system by adding the requirement of values for the holding voltage levels to satisfy conditions of firing SCR by the detected ESD event voltage and being immune to the noise, since it is

routine requirement in switching system design taught in College Electronic Design courses.

Regarding Claims 16 and 18, Ker 2 et al. disclose the plurality of diodes series connected with each P-SCR (elements D1 - Dn in Fig. 21b) and the plurality of diodes series connected with each N-SCR (elements D1 – Dn in Fig. 21a). A motivation for such modification of the primary reference was given above.

Regarding Claim 15, Ker 1 et al. disclose the P-STSCR in the ESD protection circuit including a p-type substrate with N-wells (see Fig. 2), a first N-well diffusion region and a first P^+ diffusion region in P-type substrate used as the cathode of the P-STCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 28 and 27 in Fig. 2) in the N-well (element 23 in Fig. 2) used as the anode of the P-STCR, the second P^+ diffusion region, the N-well, the P-substrate and the first N^+ diffusion region forming the first lateral SCR.

Regarding Claim 17, Ker 1 et al. disclose the circuit wherein the N-STSCR in the ESD protection circuit including a P-type substrate with N-wells (see Fig. 2), a first N^+ diffusion region and a first P^+ diffusion region in P-type substrate uses as the cathode of the N-STSCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 26 an 25 in Fig. 2) in the N-well (element 21 in Fig. 2) for use as the anode of the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

Claims 19 - 24 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 2 et al. in a view of Smith. Regarding Claim 19, Ker 2 et al. disclose most of the elements of the claim including a power-rail ESD clamp circuit connected between a Vss power terminal and a Vdd power terminal, the circuit includes: an ESD-detection circuit electrically connected between the Vss and the V DD power terminals (element 204 in Fig. 11); at least one silicon controlled rectifier (elements PCLSCR in Fig. 11) having at least one trigger node, an anode and a cathode of the SCR connected to the Vdd power and the Vss power terminals. However, they do not disclose substrate-triggered ESD protection elements. Smith discloses the substrate-triggered ESD protection elements (element 13 in Fig. 3, col. 5, line 50 – col. 6, line 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 et al. solution by adding the substrate-triggering according to Smith, because as Smith states (col. 2, lines 12 – 25), the substrate-triggering helps to lower the trigger voltage, which as well known in the art is essential for protection circuits designed for use with low supply voltage.

Regarding Claim 20, Ker 2 et al. disclose the SCR as a P-type silicon controlled rectifier and the trigger node is a P-type trigger node. As to substrate triggering, Smith discloses that feature. The motivation for modification of primary reference was given above.

Regarding Claim 21, Ker 2 et al. disclose the power-rail ESD protection circuit wherein when a positive ESD voltage pulse is applied across the Vdd power terminal

and the Vss power terminal, the ESD detection circuit generates a trigger current that flows into the P-type trigger node of the SCR to trigger the lateral SCR so that the lateral SCR enters a latch state and turns on the SCR to discharge current incurred from the positive ESD voltage pulse.

Regarding Claim 22, Ker 2 et al. disclose the SCR as a N-type silicon controlled rectifier and the trigger node is a N-type trigger node (elements NCLSCR in Fig. 10a – 10c). As to substrate triggering, Smith discloses that feature. The motivation for modification of primary reference was given above.

Regarding Claim 23, Ker 2 et al. disclose the power-rail ESD protection circuit wherein when a positive ESD voltage pulse is applied across the Vdd power terminal and the Vss power terminal, the ESD detection circuit generates a trigger current that flows into the N-type trigger node of the SCR to trigger the lateral SCR so that the lateral SCR enters a latch state and turns on the SCR to discharge current incurred from the positive ESD voltage pulse (col. 8, lines 14 – 32).

Regarding Claim 24, Ker 2 et al. disclose a plurality of diodes are series connected with the SCR (elements D1 – Dn in Fig. 21a).

Regarding Claim 33, Ker 2 et al. disclose an internal circuit as electrically connected between Vss and Vdd power terminals (shown in Fig. 16a).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 2 et al. in a view of Smith and further in a view of Russ et al. (US 6,618,233). As per Claim 25, it differs from Claim 19, rejected accordingly by it requirement of SCR being double-

triggered switch. Russ et al. disclose the SCR switch as a double-triggered silicon controlled rectifier (shown in Fig. 3) and the DT-SCR has a P-type trigger node and an N-type trigger node (points of connection of S1 and S2 switches to the SCR in Fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified The Ker 2 et al. solution by adding the double triggering feature, because as Russ et al. state (col. 1, lines 7 – 10), the double-triggering mechanism helps to achieve faster turn-on.

Regarding Claim 26, Ker 2 et al. disclose a resistor connected to the Vdd terminal and a capacitor connected to the Vss power terminals (elements R and C in Fig. 15a); and first and second inverters both electrically connected to the Vdd and the Vss power terminals (part of element 204 and element 206 in Fig. 15a). However, they do not disclose a connection of inverters to make a functional limitation of double triggering. As was discussed above, Russ et al. disclose the double triggering connection, wherein one source of positive pulse is connected to the P-type trigger node and another source of negative pulse is connected to the N-type trigger node. The inverters of Ker 2 et al. produce positive and negative pulses well suitable for triggering the P-type and N-type nodes. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 2 et al. solution by connecting one inverter to the P-type trigger node and another to the N-type trigger node, such that when an ESD voltage pulse is applied across the Vdd and the Vss power terminals, the resistor and the capacitor couple a first voltage to an input node of the first inverter so that a second voltage is output from an output node of the

first inverter to the P-type trigger node of the DT-SCR and an input node of the second inverter, and causes a third voltage to be output from the output node of the second inverter to the N-type trigger node of the DT-SCR, because as Russ et al. state (col. 1, lines 7 – 10), the double-triggering mechanism helps to achieve faster turn-on.

Claims 27 - 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 2 et al. in a view of Smith and Russ et al. and further in a view of Court Decision *In re Karlson,* 136 USPQ 184.

As per Claims 27 and 30, they differ from Claim 26, rejected accordingly, by its elimination of one of the inverters. Ker 2 et al. disclose the first and the second devices of the claim as the resistor and capacitor (elements R and C in Fig. 15a). They further disclose the inverter (element 206 in Fig. 15a). With elimination of the first inverter directly coupled to the RC elements, the output pulse of the RC element can be directly coupled to the P-type trigger node, while the output of the inverter to the N-type trigger node. Adding or omitting of one of the inverters in a group of cascade-connected inverters is a routine step in the switching systems design. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 2 et al. solution by omitting one of the cascade-connected inverters and connecting the RC element output directly to the P-type trigger node, because as Court Decision states, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art.

Regarding Claims 28, 29, 31 and 32,Ker 2 et al. disclose the first electrical device as being zener diode and the second electrical device as a resistor (elements Diode and R in Fig. 16e). They further disclose the first electrical device as a diode string (elements Diode String in Fig. 16b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the RC and diode-resistor combinations as a part of the ESD detection circuit, since they are commonly used for that purpose.

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 3 et al. (US 6,144,542). Regarding Claim 44, Ker 3 et al. disclose an ESD-connection circuit for use in separated power rails, the separated power rails including a first Vss and a first Vdd power terminals (Vdd1 and Vss1 in Fig. 3), a second Vss and a second Vdd power terminals (Vdd2 and Vss2 in Fig. 3), a first core circuit connected between the first Vdd power terminal and the first Vss power terminal (circuit 1 in Fig. 2), a second core circuit connected between the second Vdd power terminal and the second Vss power terminal (circuit 2 in Fig. 3), the ESD-connection circuit including: at least one ESD-detection circuit (ESD Detection Circuit in Fig. 11); a first sub ESD-connection circuit, a second sub ESD-connection circuit, a third sub ESD-connection circuit, and a fourth sub ESD-connection circuit (all are shown as elements A in Fig. 3, col. 5, lines 35 – 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 3 et al. circuit by introducing the ESD-detection circuit according to Ker 3 et al., because as well known in the art, it increases

sensitivity and eventually a speed of reaction and reliability of the ESD protection devices.

Claims 35 - 43, 45 – 47, 49, 50 and 51are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 3 et al. in a view of Smith. As was stated above Ker 3 et al. disclose all the elements of Claims 34 and 44. They further disclose a lateral silicon controlled rectifier (SCR) having at least one trigger node (elements PCLSCR in Fig. 9). However, regarding Claims 35 and 45, they do not disclose a substrate-triggered silicon controlled rectifier (STSCR) having a lateral silicon controlled rectifier (SCR) and at least one trigger node.

Smith discloses the substrate-triggered ESD protection elements (element 13 in Fig. 3, col. 5, line 50 – col. 6, line 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 3 et al. solution by adding the substrate-triggering according to Smith, because as Smith states (col. 2, lines 12 – 25), the substrate-triggering helps to lower the trigger voltage, which as well known in the art is essential for protection circuits designed for use with low supply voltage.

Regarding Claims 36, 37,46 and 47, Ker 3 et al. disclose an SCR as a P-type silicon controlled rectifier (PCLSCR) and the trigger node is a P-type trigger node (shown in Fig. 9). They further disclose an N-type silicon controlled rectifier (NCLSCR) and the trigger node is an N-type trigger node (shown in Fig. 10). As to the substrate triggering, it was addressed above.

Regarding Claims 39 and 49, Ker 3 et al. disclose a plurality of diodes series connected with the SCR's (elements D1 – Dn in Fig. 10).

Regarding Claims 40, 41 and 43, Ker 3 et al. disclose an ESD-connection circuit for use in separated power rails, the separated power rails including a first Vdd power terminal (Vdd1 in Fig. 3), and a second Vdd power terminal (Vdd2 in Fig. 3), the ESD-connection circuit including: a first sub power-rail ESD-connection circuit, a second sub power-rail ESD-connection circuit, and a third sub-power rail ESD-connection circuit (all are shown as elements B in Fig. 3, col. 5, lines 35 – 42). The sub power-rail ESD clamp circuit is connected between the first Vdd and Vss power terminals and between the second Vdd and Vss power terminals (elements B in Fig. 3).

Regarding Claim 42, Ker 3 et al. disclose the power-rail ESD clamp circuit of claim 40 wherein the first sub power-rail ESD clamp circuit is electrically connected between the first Vdd power terminal and the second Vdd power terminal (elements A in Fig. 3).

As per Claims 50 - 53, they introduce requirement of SCR's interconnecting different power supply lines and being connected between first and second Vdd lines and the second and the first Vss lines. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have been modified the Ker 3 et al. Fig. 2 circuit by replacing the diode strings by SCR elements according to Fig. 8 of Ker 3 et al., because the sub ESD connection circuits are replacement for upper and bottom

strings of diodes (elements 500 in Fig. 2), they are to be connected between different power supplies, i.e. the first and the second Vdd lines in the higher voltage supply line and between the second and the first.

Regarding Claims 54 and 55, Ker 3 et al. disclose the ESD detection circuit being connected between the first Vdd and Vss power terminals (Fig. 9).

Claims 38 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 3 et al. in a view of Smith and further in a view of Russ et al. Claims 38 and 48 require SCR being a double-triggered switch. Russ et al. disclose the SCR switch as a double-triggered silicon controlled rectifier (shown in Fig. 3) and the DT-SCR has a P-type trigger node and an N-type trigger node (points of connection of S1 and S2 switches to the SCR in Fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 3 et al. solution by adding the double triggering feature, because as Russ et al. state (col. 1, lines 7 – 10), the double-triggering mechanism helps to achieve faster turn-on.

Conclusion

The prior art made of record not relied upon is considered pertinent to applicant's disclosure: US 6,411,485, US 5,651,577, US 6,628,493, US 5,400,202, US 6,618,230.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by

telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone number for organization where this application or proceedings is assigned is (703) 972-9306 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
10/13/2003